Examiner's Amendment

1. An examiner's amendment to the record appears below. Should the changes and/or additions be unacceptable to applicant, an amendment may be filed as provided by 37 CFR 1.312. To ensure consideration of such an amendment, it MUST be submitted no lather than the payment of the issue fee.

2. Authorization for this examiner's amendment was given in a telephone interview with Mr. Sumit Bhattacharya, (Registration number: 51,469), on 10/8/08.

3. The specification filed on 1/15/2002 has been amended as follows:

(I) page 7, lines 7, 10 and 11, replace “device 15” with - - medium 15 - -.

4. The claims had been amended as follow:

1. An in-order multi-threading processor, comprising:

a first instruction fetch unit to receive a first thread and a second instruction fetch unit to receive a second thread;

an execution unit to execute said first thread and said second thread in parallel;

a multi-thread scheduler coupled to said first instruction fetch unit, said second instruction fetch unit, and said execution unit, wherein said multi-thread scheduler is to determine the width of said execution unit;

wherein said multi-thread scheduler unit determines whether said execution unit is to execute said first thread and said second thread in parallel depending on the width of said execution unit; and

wherein said first thread and said second thread are compiled to have instruction level parallelism.

2-4. Cancelled

5. An in-order multi-threading processor as recited in claim ~~2~~ 1, wherein said execution unit executes a third thread and a fourth thread in series.

6. Cancelled

7. An in-order multi-threading processor as recited in claim ~~6~~1, further comprising:

a first instruction decode unit coupled between said first instruction fetch unit and said multi-thread scheduler; and

a second instruction decode unit coupled between said second instruction fetch unit and said multi-thread scheduler.

8. An in-order multi-threading processor as recited in claim ~~4~~ 1, wherein said execution unit executes only two threads in parallel.

9. A computer implemented method, comprising:

determining whether an in-order multi-threading processor is wide enough to execute a first thread and a second thread in parallel;

executing said first thread and said second thread in parallel if said in-order multi- threading processor is wide enough to execute said first thread and said second thread in parallel;

executing said first thread and said second thread in series if said in-order multi-threading processor is not wide enough; and

compiling the first thread and the second thread, wherein the first thread and the second thread have instruction level parallelism.

10-12. Cancelled

13. The method as recited in claim ~~12~~ 9, wherein said multi- threading processor executes only two threads in parallel.

14. The method as recited in claim 13, further comprising:

fetching said first thread and said second thread; and

decoding said first thread and said second thread.

15. A set of instructions residing in a storage medium, said set of instructions

to be executed by an in-order multi-threading processor for searching data comprising:

determining whether said in-order multi-threading processor is wide enough to execute a first thread and a second thread in parallel;

executing said first thread and said second thread in parallel if said multi-threading processor is wide enough to execute said first thread and said second thread in parallel;

comprising executing said first thread and said second thread in series if said in-order multi-threading processor is not wide enough; and

compiling said first thread and said second thread, wherein said first thread and said second thread have instruction level parallelism.

16-18. Cancelled

19. A set of instructions as recited in claim ~~18~~ 15, wherein said in-order multi-threading processor executes only two threads in parallel.

20. A set of instructions as recited in claim 19, further comprising:

fetching said first thread and said second thread; and

decoding said first thread and said second thread.

21. A system comprising:

a memory to store a set of instructions;

an in-order processor coupled to the memory to execute said set of instructions,

said in-order processor with a first instruction fetch unit to receive a first thread, a second instruction fetch unit to receive a second thread, an execution unit to execute said first thread and said second thread, and a multi-thread scheduler coupled to said first instruction fetch unit, said second instruction fetch unit, and said execution unit, wherein said multi-thread scheduler is to determine the width of said execution unit; ~~and~~

wherein said multi-thread scheduler unit determines whether said execution unit is to execute said first thread and said second thread in parallel depending on the width of said execution unit; and

wherein said first thread and said second thread are compiled to have instruction level parallelism.

22-23. Cancelled

24. The system of claim ~~22~~ 21 wherein said execution unit executes said first thread and said second thread in parallel.

25. The system of claim ~~22~~ 21 wherein said execution unit executes said first thread and said second thread in series.

26. Cancelled

27. The system of claim ~~26~~ 21 further comprising:

a first instruction decode unit coupled between said first instruction fetch unit and

said multi-thread scheduler; and

a second instruction decode unit coupled between said second instruction fetch unit and said multi-thread scheduler.

28. The system of claim 24, wherein said execution unit executes only two threads in parallel.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to CAMQUY TRUONG whose telephone number is (571)272-3773. The examiner can normally be reached on 9:00am - 5:30pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Meng Ai An can be reached on (703)305-9678. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Meng-Ai An/
Supervisory Patent Examiner, Art Unit 2195

Camquy Truong

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